



Address Accessible Memories

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Background Module4

- Memory System
 - Memory Requirements for a Computer
 - An internal storage medium to store the intermediate as well as the final results,
 - An external storage medium to store input information, and
 - An external storage medium to store permanent results for future

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- Memory System
 - Different parameters can be used in order to classify the memory systems.
 - In the following we will use the **access mode** in order to classify memory systems
 - Access mode is defined as the way the information stored in the memory is accessed.

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- Memory System — Access Mode
 - Address Accessible Memory: Where information is accessed by its address in the memory space.
 - Content Addressable Memory: Where information is accessed by its contents (or partial contents).

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- Memory System — Access Mode
 - Within the scope of address accessible memory we can distinguish several sub-classes;
 - **Random Access Memory** (RAM): Access time is independent of the location of the information.
 - **Sequential Access Memory** (SAM): Access time is a function of the location of the information.
 - **Direct Access Memory** (DAM): Access time is partially independent of and partially dependent on the location of the information.

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- Memory System — Access Mode
 - Even within each subclass, we can distinguish several sub subclasses.
 - For example within the scope of Direct Access Memory we can recognize different groups:
 - Movable head disk,
 - Fixed head disk,
 - Parallel disk

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- Memory System
 - **Movable head disk**: Each surface has just one read/write head. To initiate a read or write, the read/write head should be positioned on the right track first — **seek time**.
 - Seek time is a mechanical movement and hence, relatively, very slow and time consuming.

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- Memory System
 - **Fixed head disk:** Each track has its own read/write head. This eliminates the seek time. However, this performance improvement comes at the expense of cost.

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- Memory System
 - **Parallel disk**: To respond the growth in performance and capacity of semiconductor, secondary storage technology, introduced **RAID** — **R**edundant **A**rray of **I**nexpensive **D**isks.
 - In short RAID is a large array of **small independent disks** acting as a single high performance logical disk.

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- Memory System — RAID
 - RAID increases the performance and reliability.
 - Data Striping
 - Redundancy

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- Memory System — RAID
 - Concept of **data striping** (distributing data transparently over multiple disks) is used to allow parallel access to the data and hence to improve disk performance.
 - In data striping, the data set is **partitioned** into equal size segments, and segments are distributed over multiple disks.
 - The size of segment is called the **striping unit**.

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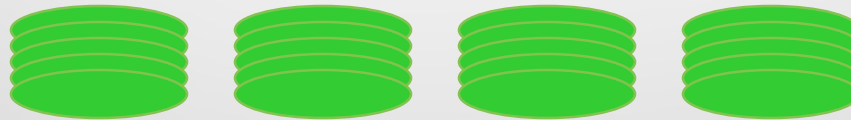
- Memory System — RAID
 - **Redundant information** allows reconstruction of data if a disk fails. There are two choices to store redundant data:
 - Store redundant information on a small number of separate disks — **check disks**.
 - Distribute the redundant information **uniformly** over all disks.
 - Redundant information can be an exact duplicate of the data or we can use a **Parity scheme** — additional information that can be used to recover from failure of any one disk in the array.

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- Memory System — RAID
 - Level 0: Striping without redundancy
 - Offers the best write performance — no redundant data is being updated.
 - Offers the highest Space utilization.
 - Does not offer the best read performance.

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- Memory System — RAID
 - Level 0



Non-redundant RAID

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- Memory System — RAID
 - Level 1: Mirrored — Two identical copies
 - Each disk has a mirror image.
 - Is the most expensive solution — space utilization is the lowest.
 - Parallel reads are allowed.
 - Write involves two disks, in some cases this will be done in sequence.
 - Maximum transfer rate is equal to the transfer rate of one disk — No striping.

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- Memory System — RAID
 - Level 1



Original Disks

Mirrored Disks

Mirrored

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- Memory System — RAID
 - Level 0 + 1: Striping and Mirroring
 - Parallel reads are allowed.
 - Space utilization is the same as level 1.
 - Write involves two disks and cost of write is the same as Level 1.
 - Maximum transfer rate is equal to the aggregate bandwidth of the disks.

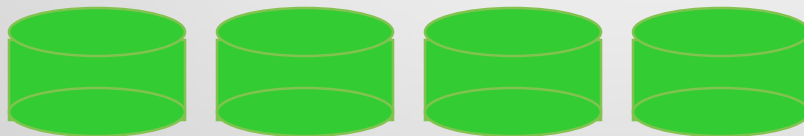
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- Memory System — RAID
 - Level 2: Error Correcting Codes
 - The striping unit is a single bit.
 - Hamming coding is used as a redundancy scheme.
 - Space utilization increases as the number of data disks increases.
 - Maximum transfer rate is equal to the aggregate bandwidth of the disks — Read is very efficient for large requests and is bad for small requests of the size of an individual block.

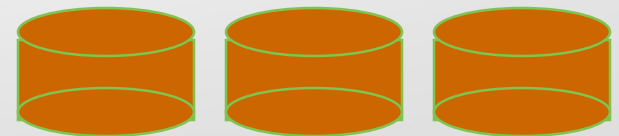
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- Memory System — RAID

- Level 2



Data Disks



Coded Information

Error Correcting Codes

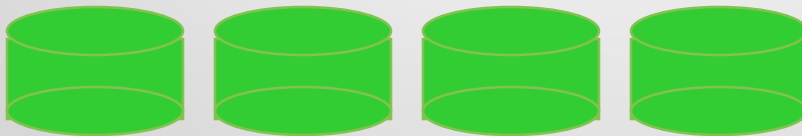
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- Memory System — RAID
 - Level 3: Bit Interleaved Parity
 - The striping unit is a single bit.
 - Unlike the level 2, the check disk is just a single parity disk, and hence it offers a higher space utilization than level 2.
 - Write protocol is similar to level 2 — read-modify-write cycle.
 - Similar to level 2, can process one I/O at a time — each read and write request involves all disks.

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- Memory System — RAID

- Level 3



Data Disks

Parity Disk

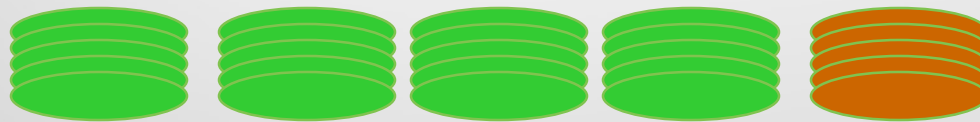
Bit Interleaved Parity

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- Memory System — RAID
 - Level 4: Block Interleaved Parity
 - The striping unit is a disk block.
 - Read requests of the size of a single block can be served just by one disk.
 - Parallel reads are possible for small requests, large requests can utilize full bandwidth.
 - Write involves modified block and check disk.
 - Space utilization increases with the number of data disks.

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- Memory System — RAID
 - Level 4



Data Disks

Parity Disk

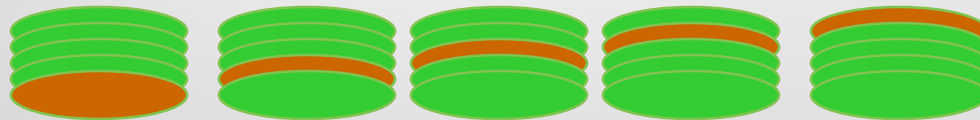
Block Interleaved Parity

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- Memory System — RAID
 - Level 5: Block Interleaved Distributed Parity
 - Parity blocks are uniformly distributed among all disks. This eliminates the bottleneck at the check disk.
 - Several writes can be potentially done in parallel.
 - Read requests have a higher level of parallelism.

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- Memory System — RAID
 - Level 5



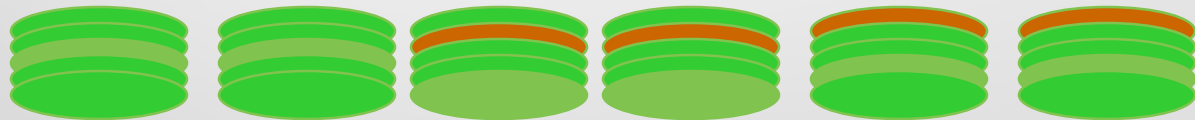
Block Interleaved Distributed Parity

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- Memory System — RAID
 - Level 6: P+Q Redundancy
 - Can tolerate higher level of failure than level 2.
 - It requires two check disks and similar to level 5, redundant blocks are uniformly distributed at the block level over the disks.
 - For small and large read requests, and large write requests, the performance is similar to level 5.
 - For small write requests, it behaves the same as level 2.

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- Memory System — RAID
 - Level 6



P+Q Redundancy

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Type	Striping	Redundancy	Space	Read	Write
RAID 0	Bit or block	No	100%	Parallel	Fastest
RAID 1	No	Mirroring	50%	Several reads	One write at a time
RAID 10	Bit or block	Mirroring	50%	Same as Raid 0	Same as Raid 1
RAID 2	Single Bit	Hamming code	57%	Bad for small #of blocks Good for large #of blocks	All disks are involved
RAID 3	Single Bit	Parity	80%	Same as Raid 2	Same as Raid 2
RAID 4	Block	Parity	80%	Overlapping several reads	No overlapping, one data and parity disks are involved
RAID 5	Block	Parity	80%	Higher than Raid 4	Overlapping several writes
RAID 6	Block	Reed-Solomon	66%	Higher than Raid 5	Same as Raid 5

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- Memory System — RAM
 - Random access memory can also be grouped into different classes
 - Read Only Memory (ROM)
 - Programmable ROM
 - Erasable Programmable ROM (EPROM)
 - Electrically Alterable ROM (EAROM)
 - Flash Memory

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- Memory System — RAM
 - Read/Write Memory (RWM)
 - Static RAM (SRAM)
 - Dynamic RAM (DRAM)
 - Synchronous DRAM
 - Double-Data-Rate SDRAM
 - Volatile/Non-Volatile Memory
 - Destructive/Non-Destructive Read Memory

Background Module4

- Memory System
 - Within the scope of Random Access Memory we are concerned about two major issues:
 - **Access Gap**: Is the difference between the CPU cycle time and the main memory cycle time.
 - **Size Gap**: Is the difference between the size of the main memory and the size of the information space.

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- Memory System
 - Within the scope of Random Access Memory we are concerned about two major issues:
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- Memory System
 - Within the scope of the memory system, the goal is to design and build a system with low cost per bit, high speed, and high capacity. In other words, in the design of a memory system we want to:
 - Match the rate of the information access with the processor speed.
 - Attain adequate performance at a reasonable cost.

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- Memory System
 - The appearance of a variety of hardware as well as software solutions represents the fact that in the worst cases the trade-off between **cost**, **speed**, and **capacity** can be made more attractive by combining different hardware systems coupled with special features — **memory hierarchy**.

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- Memory System — Access gap
 - Access gap problem was created by the advances in technology. In fact in early computers, such as IBM 704, CPU and main memory cycle time were identical — 12 μ sec.
 - IBM 360/195 had the logic delay of 5 η sec per stage, a CPU cycle time of 54 η sec and a main memory cycle time of .756 μ sec.
 - CDC 7600 had CPU and main memory cycle times of 27.5 η sec and .275 μ sec, respectively.

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- Access gap
 - How to reduce the access gap bottleneck:
 - Software Solutions:
 - Devise algorithmic techniques to reduce the number of accesses to the main memory.
 - Hardware Solutions:
 - Reduce the access gap.
 - Advances in technology
 - Interleaved memory
 - Application of registers
 - Cache memory

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- Access gap — Interleaved Memory
 - A memory is n -way interleaved if it is composed of n independent modules, and a word at address i is in module number $i \bmod n$.
 - This implies consecutive words in consecutive memory modules.
 - If the n modules can be operated independently and if the memory bus line is time shared among memory modules then one should expect an increase in bandwidth between the main memory and the CPU.

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- Access gap — Interleaved Memory
 - Dependencies in the programs — branches and randomness in accessing the data will degrade the effect of memory interleaving.

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- Access gap — Interleaved Memory
 - To show the effectiveness of memory interleaving, assume a pure sequential program of m instructions.
 - For a conventional system in which main memory is composed of a single module, the system has to go through m -fetch cycles and m -execute cycles in order to execute the program.
 - For a system in which main memory is composed of n modules, the system executes the same program by executing $\lceil m/n \rceil$ -fetch cycles and m -execute cycles.

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- Access gap — Interleaved Memory
 - The concept of modular memory can be traced back to the design of the so-called **Harvard-class machines**, where the main memory was composed of two modules: namely, program memory and data memory.

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- Access gap — Interleaved Memory
 - It was in the design of the ILLIAC II System, where the concept of the interleaved memory was introduced.
 - In this machine, the memory was composed of two units. The even addresses generated by the CPU were sent to the module 0 and the odd addresses were directed to the module 1.