CS 5803
Introduction to High Performance Computer Architecture: Content Accessible Memories

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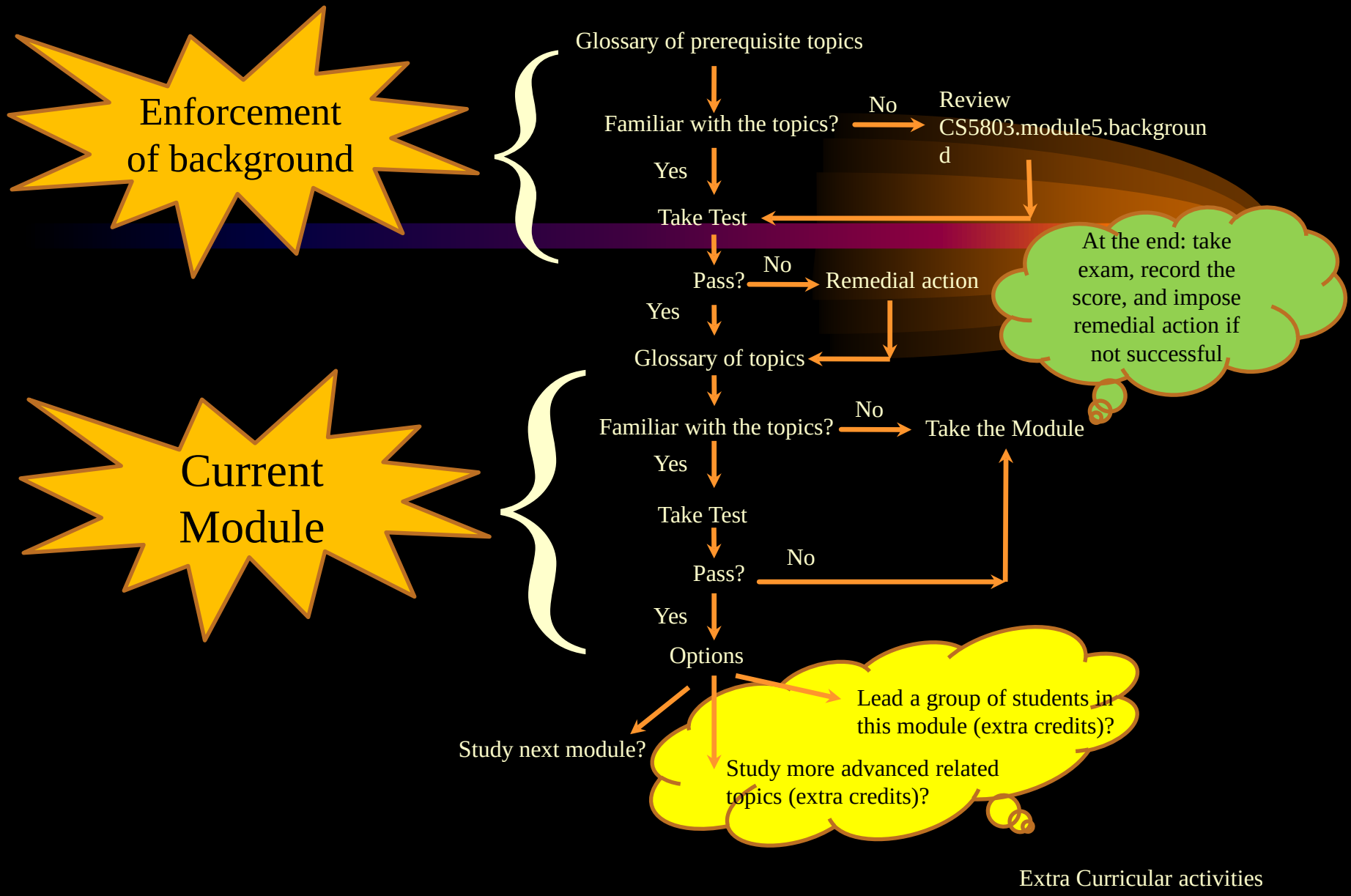
- Outline
  - Associative Memory:
    - Definition
    - Basic Operations
    - Advantages/Disadvantages
  - Basic components of associative memory
  - Different classes of associative memory
  - A sample hardware design
  - Associative algorithms
  - Application of associative memory

Note, this unit will be covered in one week. In case you finish it earlier, then you have the following options:

1) Take the early test and start CS5803.module6
2) Study the supplement module (supplement CS5803.module5)
3) Act as a helper to help other students in studying CS5803.module5

Note, options 2 and 3 have extra credits as noted in course outline.


Enforcement of background
Glossary of prerequisite topics
Familiar with the topics?
No
Review CS5803.module5.background
Yes
Take Test
Pass?
No
Remedial action
Yes
Glossary of topics
At the end: take exam, record the score, and impose remedial action if not successful
Current Module
Familiar with the topics?
No
Take the Module
Yes
Take Test
Pass?
No
Yes
Options
Study next module?
Lead a group of students in this module (extra credits)?
Study more advanced related topics (extra credits)?
Extra Curricular activities

- Memory System
  - If you recall, based on accessing mode we distinguished two classes of memory systems:
    - Address accessible Memory, and
    - Content addressable Memory
  - In the last module, we concentrated on address accessible memory. This module concentrates on the content addressable memory.

- Associative Memory
  - A Content Addressable Memory is defined as a collection of storage elements which are accessed in parallel on the basis of data contents rather than by specific address or location.

- Associative Memory
  - Each associative cell should have hardware capability to store and search its contents against the data which is broadcast by the control unit, and indicate a match or mismatch by the state of a flip flop.
  - Consequently, each associative cell is more expensive and larger than a random access cell.

- Associative Memory
  - A content addressable processor is a content addressable memory with the added capability to write in parallel (multi-write) into all those words indicating agreement as the result of a search.

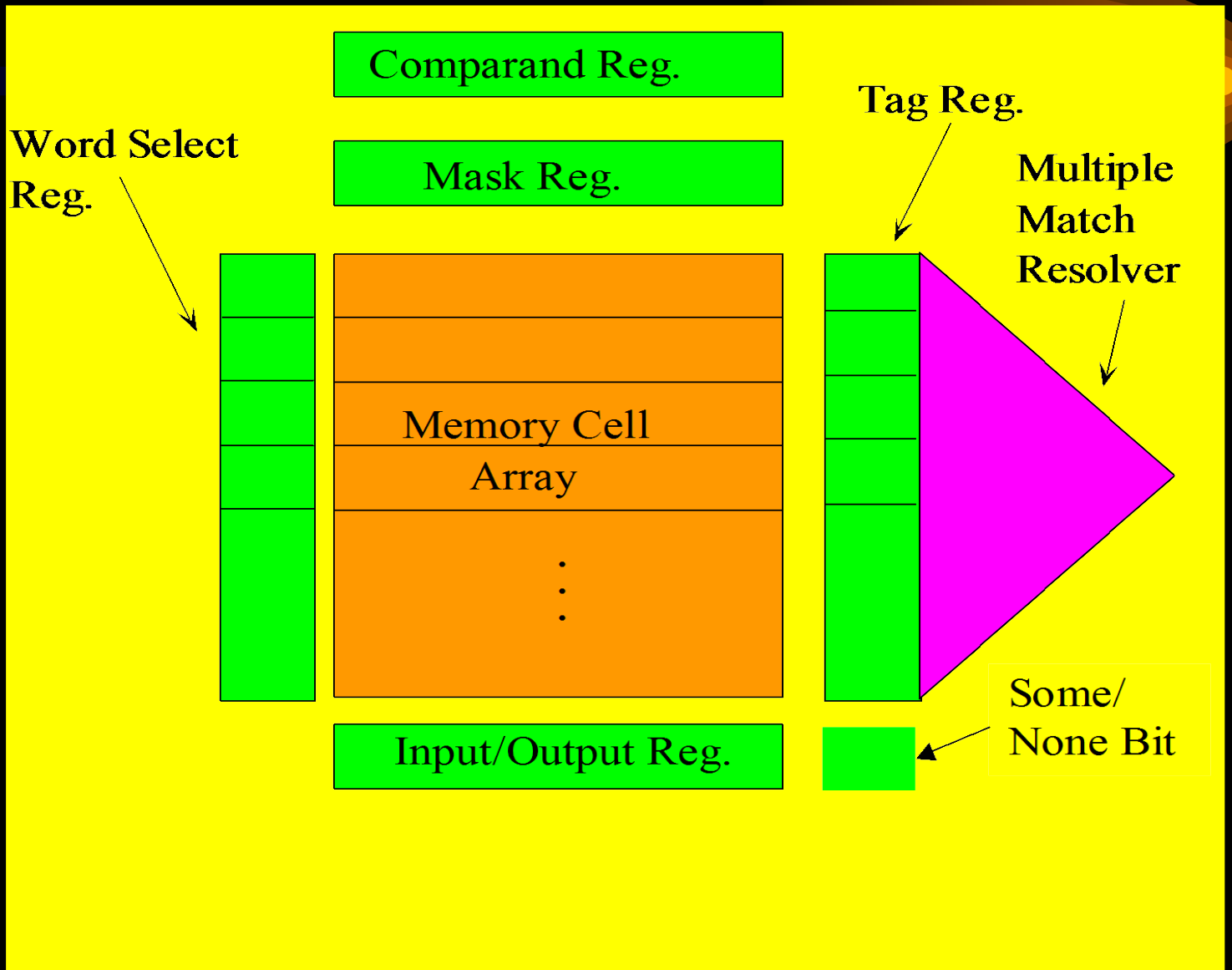
- Associative Memory
  - Based on our early definition of associative memory, then we can conclude that Read, write, and search are the basic operations in an associative memory.

- Associative Memory
  - Historically, content addressable memory was proposed in the mid 50s but the first commercial associative memory was made available in the early 70s.
  - This delay between conception and realization was due:
    - Cost,
    - Flexibility and versatility of the von Neumann concept,
    - Conservatism of the computer programmers and makers.

- Associative Memory — Advantages
  - Content addressability
  - Parallelism
  - In-place operations
    -
    -
    -

- Associative Memory — Disadvantages
  - Cost
  - Size of the basic memory cell
  - Long propagation delay
  - Input/Output operations
    -
    -
    -

- Associative Memory
  - A typical associative memory has the following components:
    - Memory array
    - Comparand register
    - Mask register
    - Match/Mismatch (response) register
    - Multiple match resolver
    - Search logic
    - Input/Output register
    - Word select register


Comparand Reg.
Tag Reg.
Word Select Reg.
Mask Reg.
Multiple Match Resolver
Memory Cell Array
Some/ None Bit
Input/Output Reg.

- Associative Memory
  - Memory Cell Array provides storage and search medium for data.
  - Comparand Register contains the data to be compared against the contents of the memory cell array.
  - Mask Register is used to mask off portions of the data words which do not participate in the operations.

- Associative Memory
  - Word Select Register is used to mask off the memory words which do not participate in the operation.
  - Match/Mismatch Register indicates the success or failure of a search operation.
  - Input/Output Buffer acts as an interface between associative memory and the outside word.

- Associative Memory
  - Multiple Match Resolver narrows down the scope of the search to a specific location in the memory cell array in a cases where more than one memory word will satisfy the search condition(s).
  - Some/None bit shows the overall search result.

- Associative Memory
  - Associative memories can be classified into four groups:
    - Fully Parallel
      - Word organized
      - Distributed logic
    - Bit-Serial Word-Parallel
    - Bit-Parallel Word-Serial
    - Block Oriented

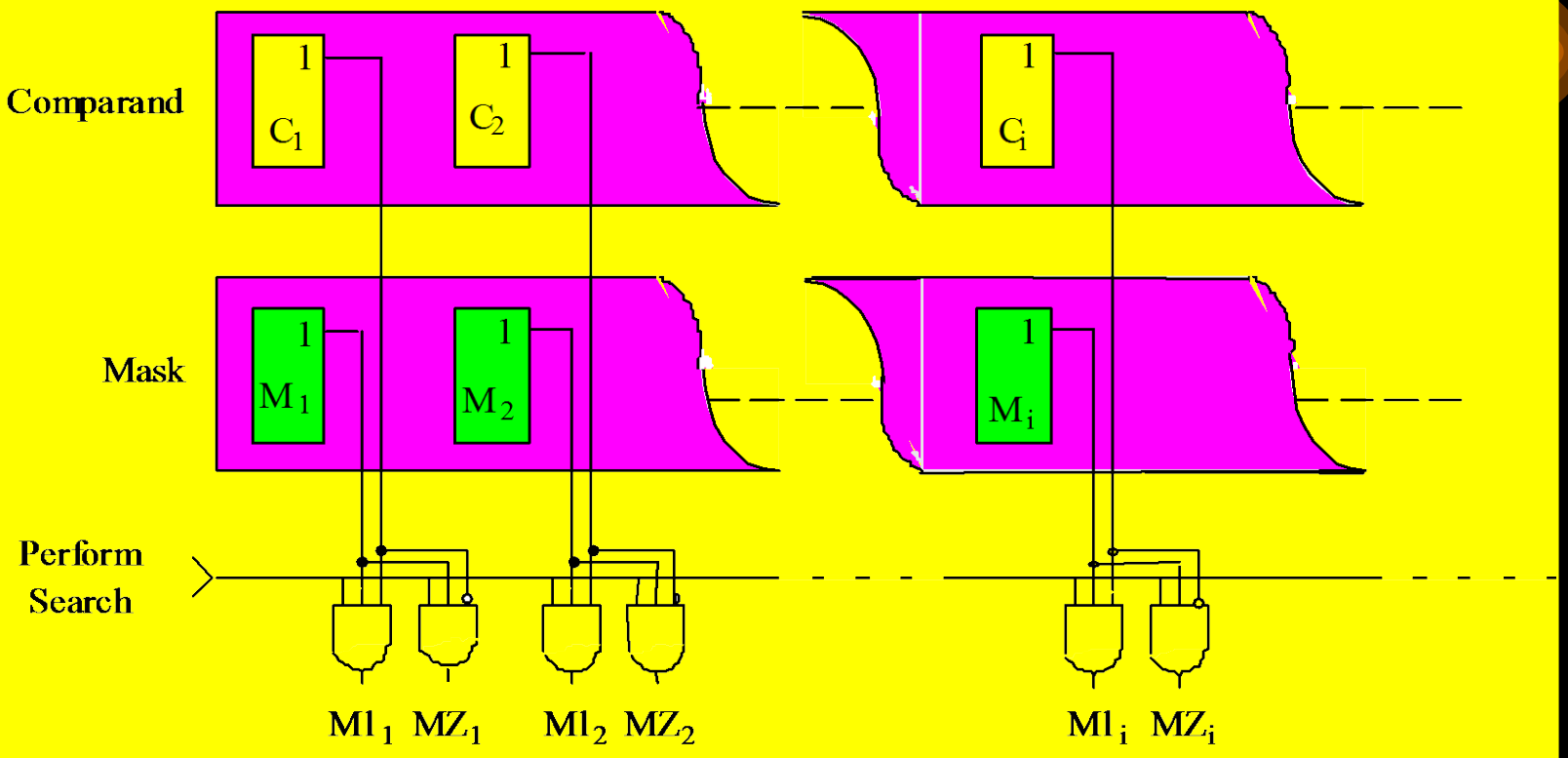
- Associative Memory — Fully Parallel
  - In this organization search circuitry is associated with every bit in the memory. This lets the entire memory be searched at the same time and provides the fastest search time of all the classifications.

- Associative Memory — Bit-Serial Word-Parallel
  - In this organization search circuitry is associated with a single bit of each word (Bit-Slice) and all the bits of each word must be shifted through its search bit to perform a search — search time is a function of the word length.

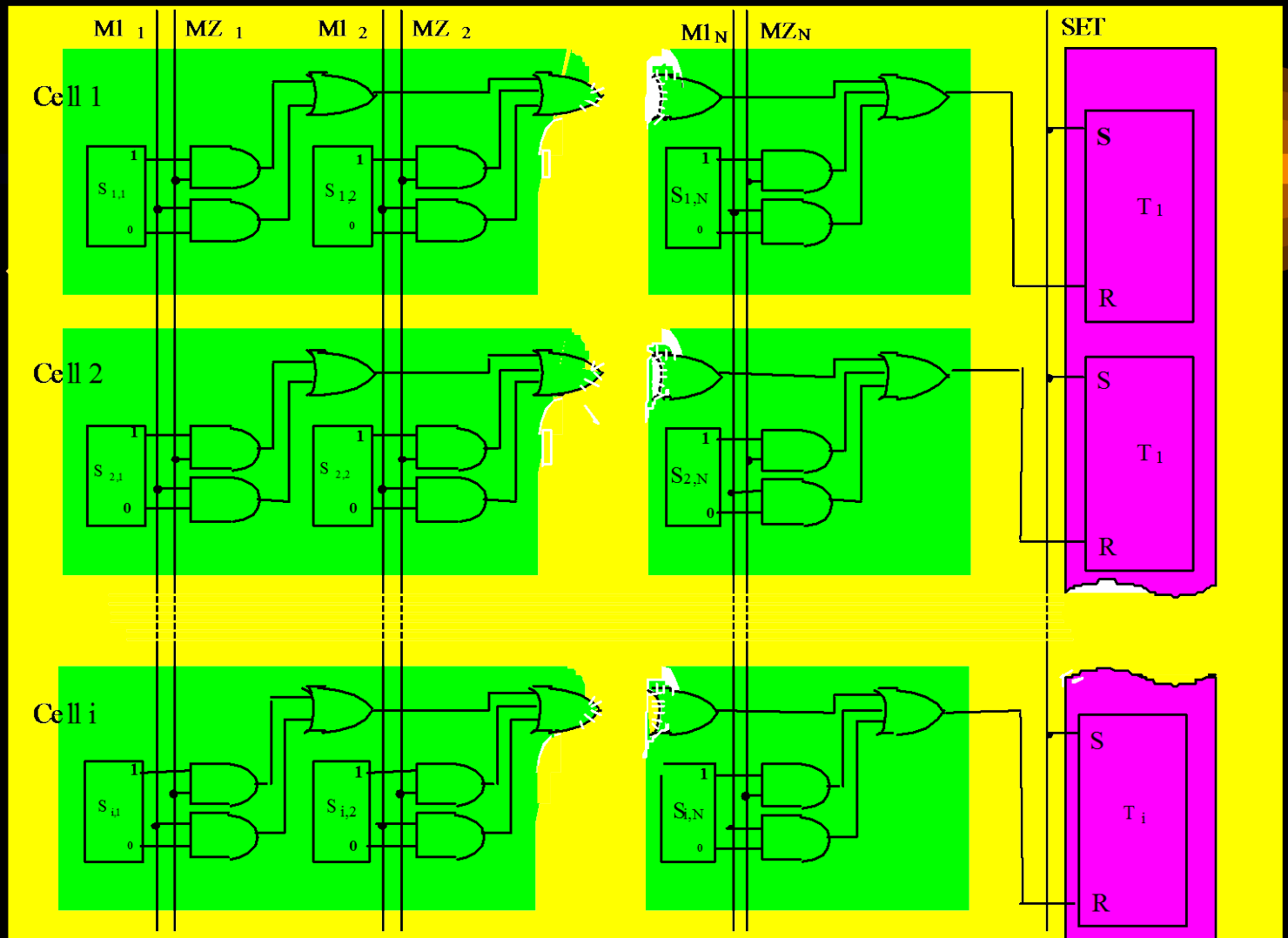
- Associative Memory — Bit-Parallel Word-Serial
  - In this approach search circuitry is associated with a single word of the memory, thereby implementing a hardware version of a standard linear search algorithm — search time depends on the number of words in the memory.

- Associative Memory — Block-Oriented
  - In this model search circuitry is associated with a block of data at the secondary storage level.
  - Block oriented associative memory was implemented by adding a processor to the read/write head of a disk which can perform associative operations on the data passing under the head.

- Associative Memory — An Example
  - N: word Length
  - K: number of the words
  - C_i: i^{th} bit of the comparand register $\forall\ 1 \leq i \leq N$
  - M_i: i^{th} bit of the mask register $\forall\ 1 \leq i \leq N$
  - S_{ji}: i^{th} bit of the j^{th} word in the memory array cell $\forall\ 1 \leq i \leq N$ and $1 \leq j \leq K$
  - T_j: j^{th} bit of the Tag register $\forall\ 1 \leq j \leq K$

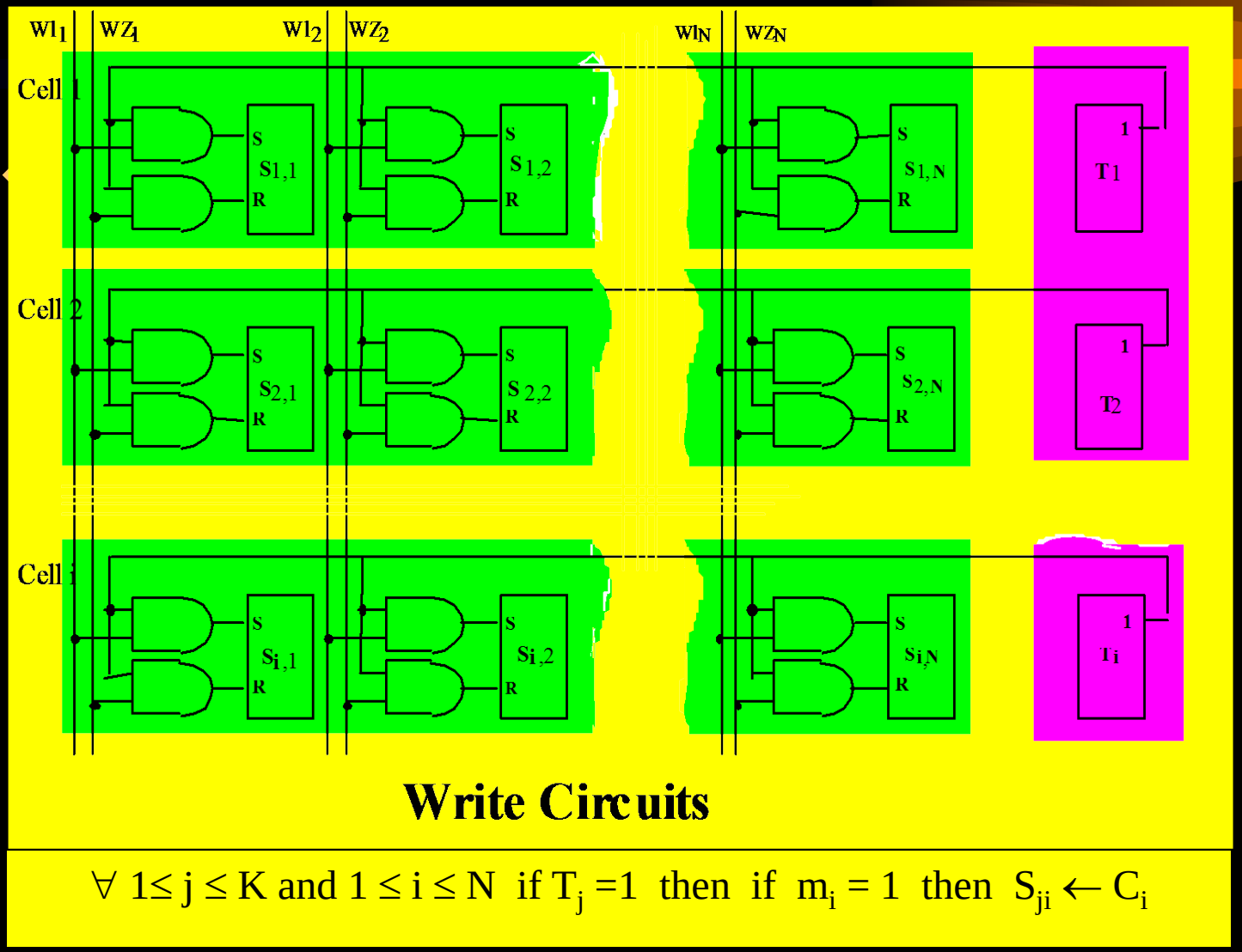


$$\forall \quad 1 \le i \le N \begin{cases} Ml_i = 1 & \text{iff} \quad M_i = C_i = 1 \\ MZ_i = 1 & \text{iff} \quad M_i = 1 \text{ and } \quad C_i = 0 \\ Ml_i = MZ_i = 0 & \text{iff} \quad M_i = 0 \end{cases}$$

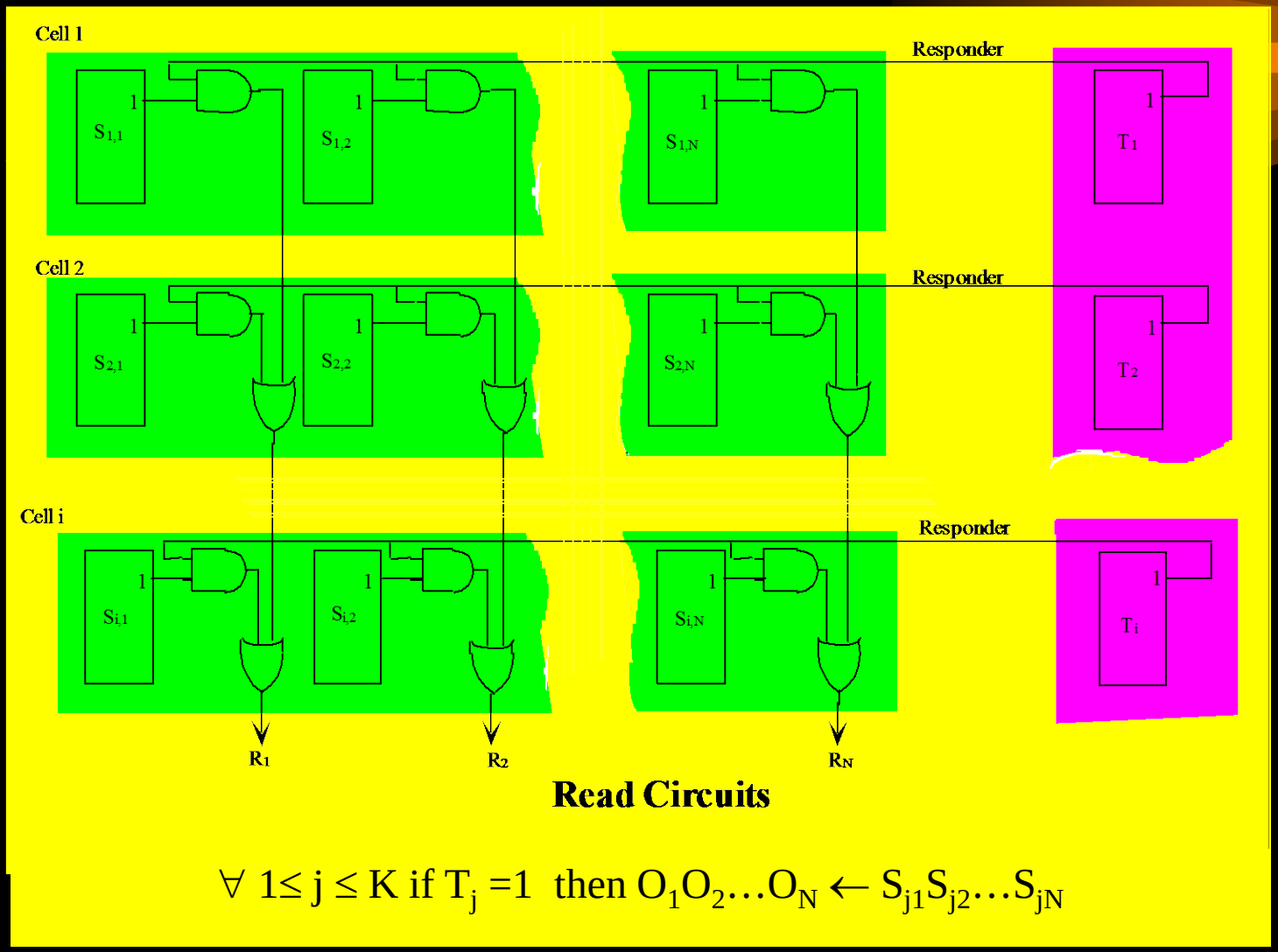


Inequality Search

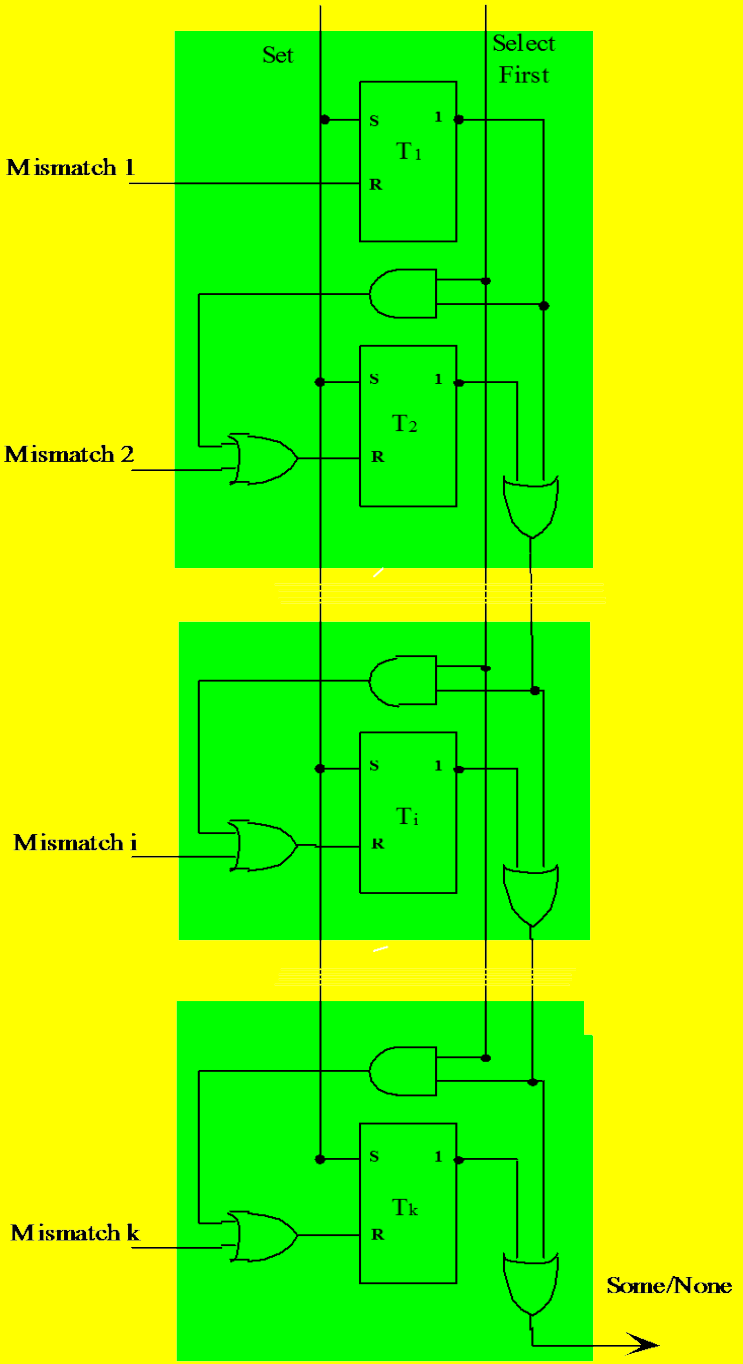
$\forall\ 1 \le j \le K$ and $1 \le i \le N$ $T_j = 0$ iff $\exists$ at least an i such that $S_{ji} \neq C_i$



$\forall\ 1 \le j \le K$ and $1 \le i \le N$ if $T_j = 1$ then if $m_i = 1$ then $S_{ji} \leftarrow C_i$



$\forall\ 1 \leq j \leq K$ if $T_j = 1$ then $O_1 O_2 \ldots O_N \leftarrow S_{j1} S_{j2} \ldots S_{jN}$

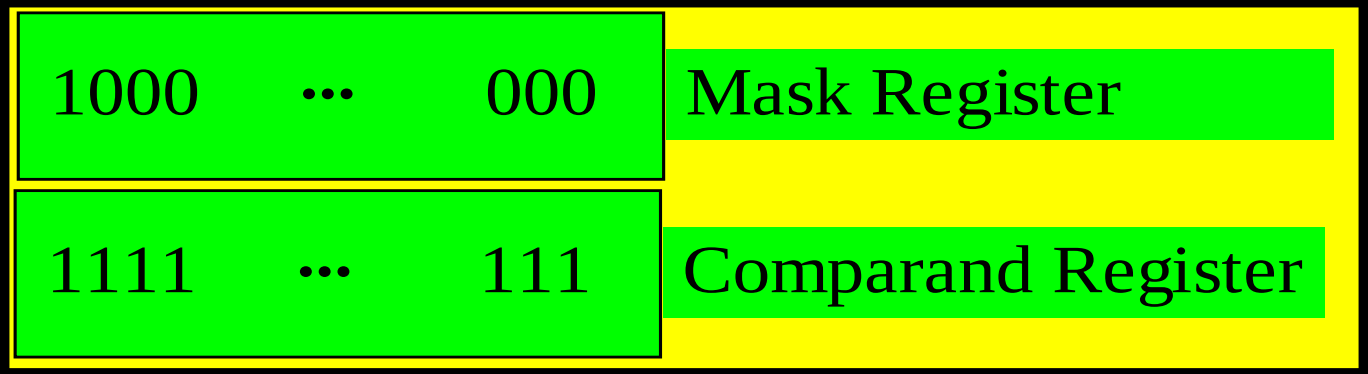


The Circuit Surrounding the Tag Bits

Some/None = 1 iff ∃ a j such that
$T_j = 1 \qquad 1 \le j \le k$

- Associative Memory — An Example
  - Find the greatest value stored in the memory.
  - Assume numbers are all positive and each word contains one number.
  - The following algorithm generates the largest value in the comparand register.

- Associative Memory — An Example
  - Initially we have:



- Associative Memory — An Example
  - 1) Set all Tag bits to zero.
  - 2) Compare for equality.
  - 3) Any response?
    - 4) Yes: any more zeros in the mask register?
      - 5) No: end of the algorithm, Stop.
      - 6) Yes: change the leftmost zero in the mask register to 1, goto step 1.
    - 7) No: change the comparand bit corresponding to the rightmost 1 in the mask register to 0, goto step 2.

1	1	1	1	1
1	0	0	0	0
1	1	0	0	0
1	0	0	0	1
0	1	1	1	1
1	1	0	0	1
1	1	1	1	0

Search on equality

1	1	1	1	1
1	1	0	0	0
1	1	0	0	0
1	0	0	0	1
0	1	1	1	1
1	1	0	0	1
1	1	1	1	0

Search on equality

1	1	1	1	1
1	1	1	0	0
1	1	0	0	0
1	0	0	0	1
0	1	1	1	1
1	1	0	0	1
1	1	1	1	0

Search on equality

1	1	1	1	1
1	1	1	1	0
1	1	0	0	0
1	0	0	0	1
0	1	1	1	1
1	1	0	0	1
1	1	1	1	0

Search on equality

1	1	1	1	1
1	1	1	1	1
1	1	0	0	0
1	0	0	0	1
0	1	1	1	1
1	1	0	0	1
1	1	1	1	0

Search on equality

1	1	1	1	0
1	1	1	1	1
1	1	0	0	0
1	0	0	0	1
0	1	1	1	1
1	1	0	0	1
1	1	1	1	0

Search on equality

- Associative Memory — An Example
  - Add 1 to the memory words.
  - Assume numbers are positive and overflow is of no concern.
  - One column of associative memory is used as a carry column.

Associative Memory — An Example

- Set $Carry_j$=1 for all words.
- For i=N to 1 do
- Mark all words as unprocessed.
- Set C_i to 0 and mask out C_k $\forall$ K $\neq$ i
- Search for equality:
- if $Carry_j$ = 1 then $S_{ji} \leftarrow$ 1 and $Carry_j \leftarrow$ 0
- Set all responses as processed.
- Set C_i = 1
- Search for Equality:
- if $Carry_j$ = 1 then $S_{j,i} \leftarrow$ 0
- End

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				0
				1
1	1	0	0	0
1	0	0	0	1
0	1	1	1	1
1	1	0	0	1
1	1	1	1	0

1
1
1
1
1

			0	
			1	
1	1	0	0	***1***
1	0	0	0	0
0	1	1	1	0
1	1	0	0	0
1	1	1	1	***1***

0
1
1
1
0

		0		
		1		
1	1	0	0	***1***
1	0	0	***1***	0
0	1	1	0	0
1	1	0	***1***	0
1	1	1	1	***1***

0
0
1
0
0

	0			
	1			
1	1	0	0	***1***
1	0	0	***1***	0
0	1	0	0	0
1	1	0	***1***	0
1	1	1	1	***1***

0
0
1
0
0

- Questions
  - Write an associative algorithm to find the smallest number in the memory.
  - Write an associative algorithm to calculate the 1^s complement of the contents of the memory words.
  - Write an associative algorithm to calculate the 2^s complement on the contents of the memory words.
  - Write an associative algorithm to partition the memory words into three sets (smaller than, equal to, and greater than) with respect to a fixed value (a).
  - Write an associative algorithm to add a fixed value to the contents of the memory words.

- Associative Memory
  - Application of associative processing in handling numeric and non-numeric data in diverse areas has been extensively addressed in the literature. This includes:
    - Memory Management and Address Mapping Operations.
    - Image Processing.
    - Design of Dataflow Machines.

- Associative Memory
  - Design of LISP Machines.
  - Design of PROLOG Machines.
  - Design of Database Machines.

- Associative Memory
  - In general, associative processing is very suitable for:
    - Massive simple arithmetic operations
    - Image processing
    - Database processing.

- Associative Memory
  - A fully parallel associative memory is very well suited to VLSI technology because of its simple, regular, and modular structure.

- Associative Memory
  - Some efforts to fabricate/develop

Year	Capacity (bit)	Cell Size λ^2	Application
1985	4-K	2652	Artificial Intelligence
1985	8-K	1080	Dataflow Processing
1986	20-K	1438	Artificial Intelligence
1987	16-K	5000	Database Processing
1988	6-K	14092	Database Processing
1988	2-K	3040	PROLOG-based Computers
1988	9-K	1656	Parallel Processing
1989	8-K	9544	Database Processing
1990	16-K	5016	Database Processing

- Associative Memory
  - Despite the advantages of associative processing, there are very few associative memories available on the market either as general purpose chips or as components in standard cell libraries for VLSI design. Two issues could have contributed to this fact:
    - perceived high cost of the associative memory, and
    - diversity of the applications.

- Associative Memory
  - At first glance, the perceived high cost of associative memory seems a valid concern. However, because of the recent advances in technology and increased functionality of associative memory such a cost increase should be acceptable.

- Associative Memory
  - As a reminder, it should be noted that each bit of a dynamic equality-search associative memory is only 1.5 times the size of a fully static random access memory cell.
  - This area penalty is more than offset by the increased functionality and parallelism of the associative memory.

- Associative Memory
  - To remedy the diversity issue one has to devise a generalized methodology to quickly produce high capacity associative chips with different functionality. This is achieved if:
    - modularity is enforced at the lowest level, and
    - an automatic and interactive design tool can be developed which designs customized associative chips.