**Solution HW#2**

1. 40

2. VCC PIN 40 and GND PIN 20

3. 32 Pins

4. 8 Pins and from 32 to 39.

5. 8 Pins and from 1 to 8.

6. 8 Pins and from 21 to 28.

7. 8 Pins and from 10 to 17.

8. Input

9. P0 (Port 0)

10. P1 (Port 1)

16. All ports are bit addressable.

17. We can manipulate a single bit without changing other bits of the port by using Setb and Clr.

19. No , since CPL works with A register and individual bits.

20.

ORG 0000H

SETB P1.2

SETB P1.5

BACK: ACALL DELAY

CPL P1.2

CPL P1.5

SJMP BACK

END

21.

ORG 0000H

SETB P2.5

SETB P1.7

SETB P1.3

BACK: ACALL DELAY

CPL P1.3

CPL P1.7

CPL P2.5

SJMP BACK

END

23.

ORG 0000H

SETB P2.7

BACK: JB P2.7, BACK

HERE: MOV A, #55H

MOV P0, A

ACALL DELAY

MOV A, #0AAH

MOV P0, A

ACALL DELAY

SJMP HERE

END

1. b is invalid , no # sign
2. a Immediate

b Direct

c Direct

d Immediate

e Direct

f Immediate

g Register

h Direct

I Register Indirect

J Register

K Register Indirect

1. Refer page Figure 5-1, and figure 5-2 on text.
2. Register bank 1 , 2 , 3 share the space with stack because by default stack starts from 08H
3. Direct
4. It copies the contents of the B register into the accumulator
5. It copies the contents of R7 of bank 3 into the accumulator

8.

ORG 0000H

PUSH 00H

PUSH 01H

PUSH 03H

POP 1FH

POP 1EH

POP 1DH

END

9. Registers R0 and R1.

19.

a) Invalid

b) Valid, bit 3 of P2

c) Valid, bit 5 of A

d) P1.0

e) bit 4 of B

f) P0.0

g) bit 3 of PSW

h) P0.7

3)

CLR PSW.3

SETB PSW.4

MOV R7, A

4)

See the class notes