**Project**

**CpE5110/CS5700**

You are expected to develop a **simulator** to mimic the behavior of SRT division technique (in a high level language).

Dividend length and divisor length are (8, 4), (12, 6), (16, 8), and (24, 12) bits, both fractions (dividend and divisor could be unnormalized). Your simulator should generate the result, execution time in term of Δt, where Δt is the delay of a basic logic gate (AND or OR). You also need to draw a plot showing the execution time vs. the operand length (in case you have more than one data set, you need to plot the average execution time).

You are expected to write a **technical report** detailing your project, generated results, and analysis of the results. Due date is April 9 (this is a firm due date).

Please make note of the following:

1. The test data will be made available on the course web site on April 2.
2. The due date of the project is firm and will not change under any circumstances.
3. Each group is expected to submit in class a hard copy of the report along, with a print-out of the simulator. The simulator is expected to be well- documented.

Please note that randomly-selected groups may be asked to demo their project and execute it on input data.

You are using carry select adder to perform addition,

Shift operation is 3Δt, and

2s complement operation is n\*Δt (n is the operand length).